CLAIMS

1. A floating gate memory cell situated on a substrate, said floating gate memory cell comprising:

a stacked gate structure situated on said substrate, said stacked gate structure being situated over a channel region in said substrate;

a recess formed in said substrate adjacent to said stacked gate structure, said recess having a sidewall, a bottom, and a depth;

a source of said floating gate memory cell situated adjacent to said sidewall of said recess and under said stacked gate structure;

a Vss connection region situated under said bottom of said recess and under said source, said Vss connection region being connected to said source;

wherein said Vss connection region being situated under said bottom of said recess causes said source to have a reduced lateral diffusion in said channel region.

2. The floating gate memory cell of claim 1 wherein said reduced lateral diffusion of said source causes a reduction in drain induced barrier lowering in said floating gate memory cell.

3. The floating gate memory cell of claim 1 wherein said recess allows a resistance of said Vss connection region to be decreased without increasing drain induced barrier lowering in said floating gate memory cell.

4. The floating gate memory cell of claim 1 wherein said sidewall of said recess is substantially perpendicular to a top surface of said substrate.

5. The floating gate memory cell of claim 1 wherein said depth of said recess is between approximately 200.0 Angstroms and approximately 500.0 Angstroms.

6. The floating gate memory cell of claim 1 wherein said stacked gate structure comprises an ONO stack situated on a floating gate.

7. The floating gate memory cell of claim 1 wherein said floating gate memory cell is a NOR-type floating gate flash memory cell.

8. A floating gate memory cell situated on a substrate, said floating gate memory cell comprising a stacked gate structure situated on said substrate, said stacked gate structure being situated over a channel region in said substrate, a recess formed in said substrate adjacent to said stacked gate structure, said recess having a sidewall, a bottom, and a depth, said floating gate memory cell being characterized in that:

a source of said floating gate memory cell is situated adjacent to said sidewall of said recess and under said stacked gate structure, a Vss connection region is situated under said bottom of said recess and under said source, said Vss connection region

being connected to said source, wherein said Vss connection region being situated under said bottom of said recess causes said source to have a reduced lateral diffusion in said channel region.

9. The floating gate memory cell of claim 8 wherein said reduced lateral diffusion of said source causes a reduction in drain induced barrier lowering in said floating gate memory cell.

10. The floating gate memory cell of claim 8 wherein said recess allows a resistance of said Vss connection region to be decreased without increasing drain induced barrier lowering in said floating gate memory cell.

11. The floating gate memory cell of claim 8 wherein said sidewall of said recess is substantially perpendicular to a top surface of said substrate.

12. The floating gate memory cell of claim 8 wherein said depth of said recess is between approximately 200.0 Angstroms and approximately 500.0 Angstroms.

13. The floating gate memory cell of claim 8 wherein said stacked gate structure comprises an ONO stack situated on a floating gate.

14. The floating gate memory cell of claim 8 wherein said floating gate memory cell is a NOR-type floating gate flash memory cell.

15. A method for fabricating a floating gate memory cell on a substrate, said method comprising steps of:

forming a heavily doped region in a source region in said substrate, said source region being situated adjacent to said stacked gate structure;

forming a recess in said heavily doped region in said substrate, said recess having a sidewall, a bottom, and a depth, said sidewall of said recess being situated adjacent to a source of said floating gate memory cell;

forming a Vss connection region under said bottom of said recess and under said source, said Vss connection region being connected to said source;

wherein forming said Vss connection region under said bottom of said recess causes said source to have a reduced lateral diffusion in said channel region.

16. The method of claim 15 wherein said reduced lateral diffusion of said source causes a reduction in drain induced barrier lowering in said floating gate memory cell.

17. The method of claim 15 wherein said recess allows a resistance of said Vss connection region to be decreased without increasing drain induced barrier lowering in said floating gate memory cell.

18. The method of claim 15 further comprising a step of performing an anneal process after said step of forming said heavily doped region and prior to said step of forming said recess.

19. The method of claim 15 wherein said sidewall of said recess is substantially perpendicular to a top surface of said substrate.

20. The method of claim 15 wherein said depth of said recess is between approximately 200.0 Angstroms and approximately 500.0 Angstroms.